

FIG. 1

Storage Media  
Disk Controller  
Memory  
Processor

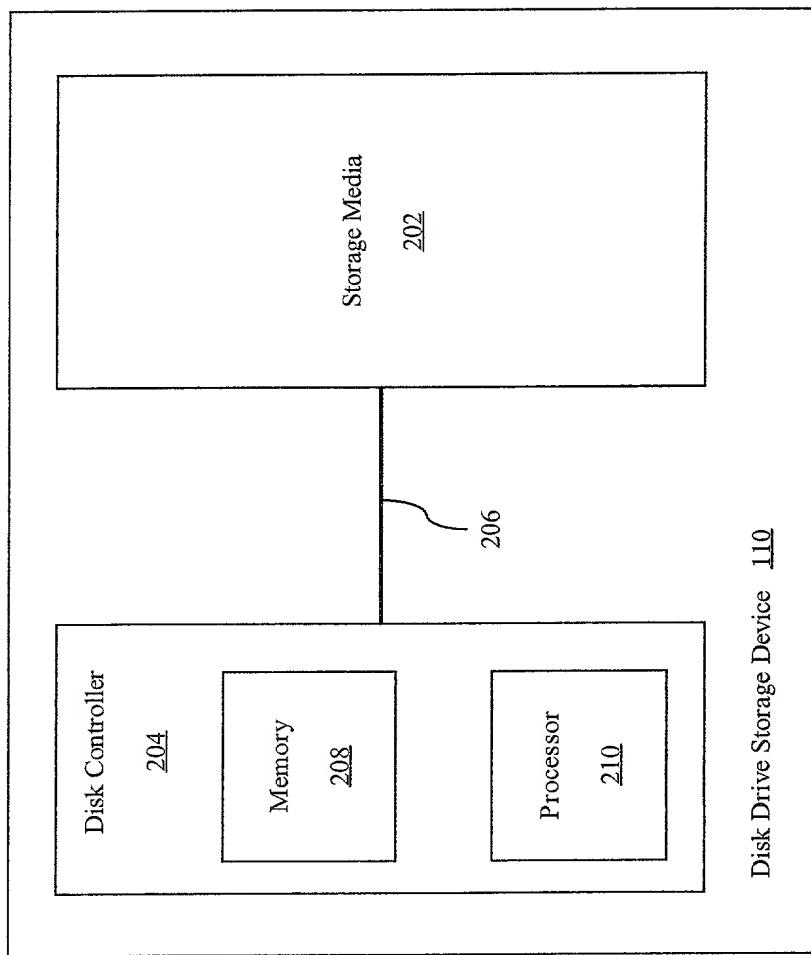
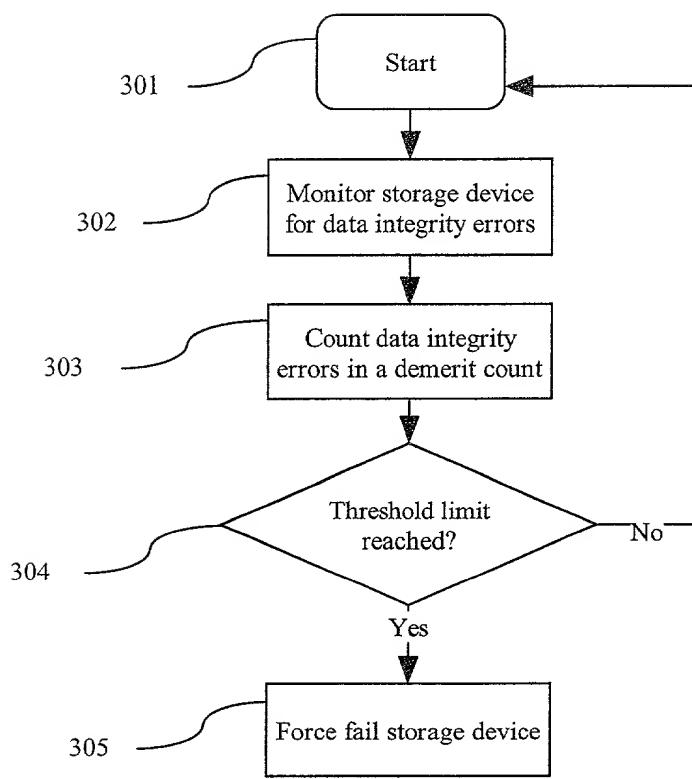


FIG. 2



**FIG. 3**

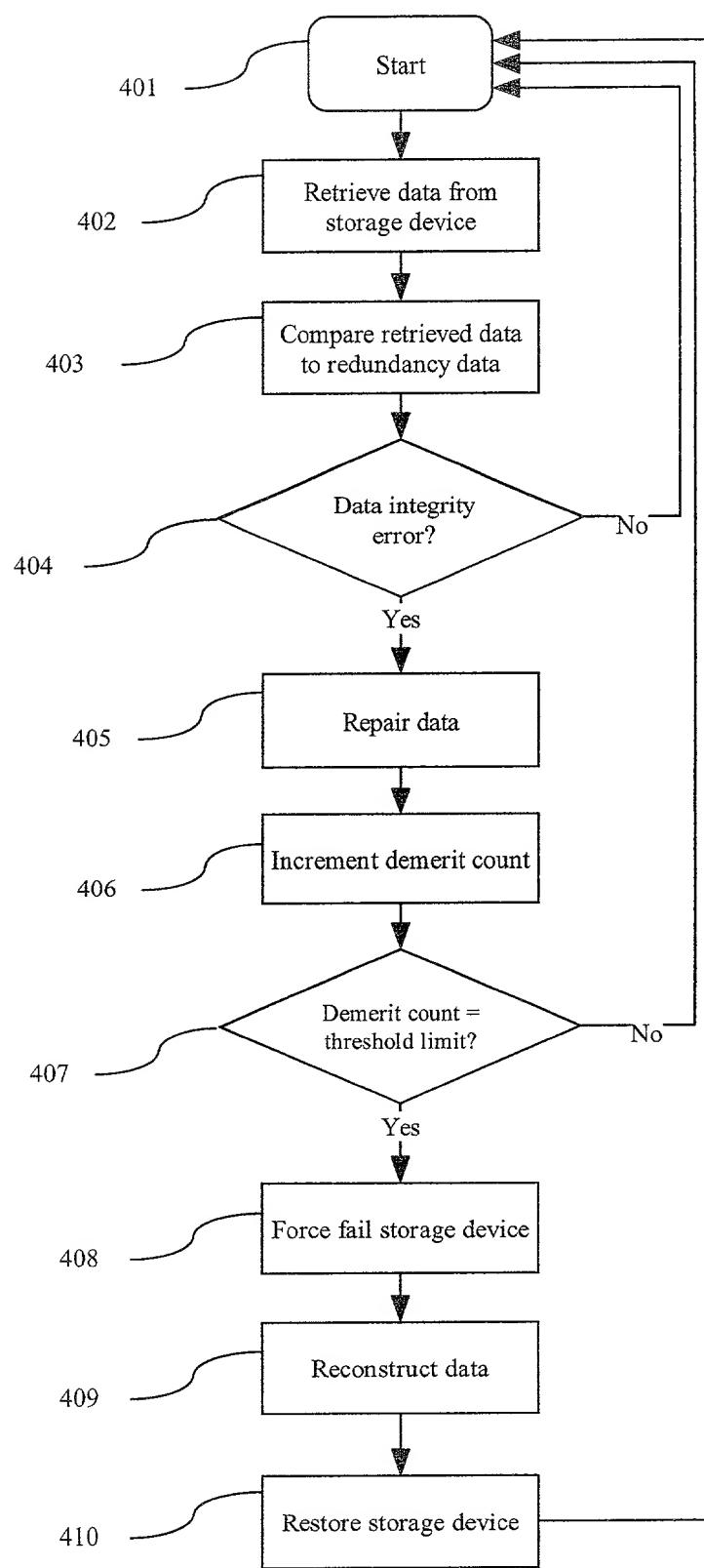
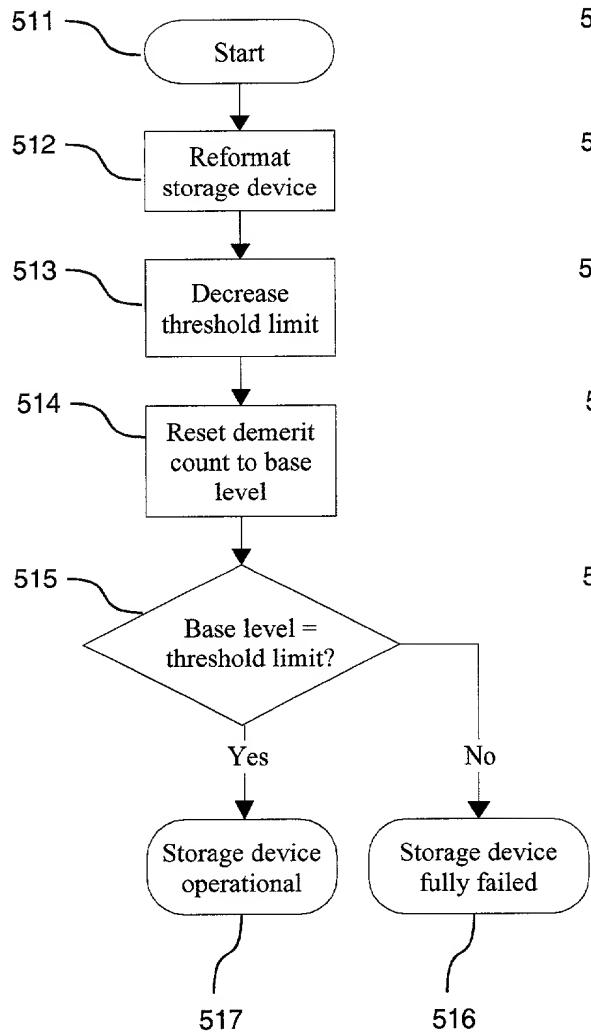
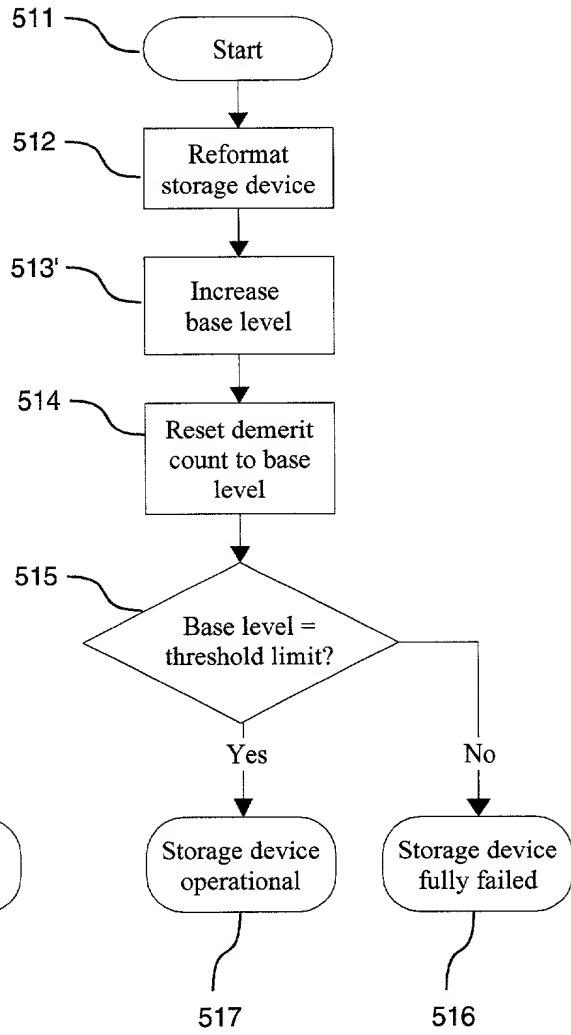


FIG. 4



**FIG.5a**



**FIG.5b**

<i>Drive #</i>	<i>Demerit Count</i>	<i>Threshold Limit</i>	<i>Base Level</i>
1	3	10	0
2	2	10	0
3	0	10	0
4	8	8	0
5	4	10	0

FIG. 6a

<i>Drive #</i>	<i>Demerit Count</i>	<i>Threshold Limit</i>	<i>Base Level</i>
1	3	10	0
2	2	10	0
3	0	10	0
4	8	10	2
5	4	10	0

FIG. 6b